IN THE SPECIFICATION

Please amend the heading at page 2, line 18 as follows:

COMMUNICATIONS SYSTEM AND METHOD FOR TRANSMITTING/RECEIVING DATA, AND INFORMATION PROCESSING APPARATUS AND METHOD FOR TRANSMITTING/RECEIVING DATA~~, AND PROGRAM~~

Please insert the following on page 1 after the Title of the Invention:

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application is a national stage application under 35 U.S.C. § 371 of International Application No. PCT/JP2004/011420, filed August 3, 2004, which claims priority from Japanese Application No. 2003-324919, filed September 17, 2003, the disclosures of which are hereby incorporated by reference herein.

BACKGROUND OF THE INVENTION

Please amend the heading at page 2, line 18 as follows:

SUMMARY ~~DISCLOSURE~~ OF THE INVENTION

Please insert the following heading before page 10, line 22:

DETAILED DESCRIPTION

Please amend the paragraph at page 19, lines 21-30 as follows:

Data frames transmitted from the synchronization master apparatus 12 are accumulated at the network interface 212. Under the control of the CPU 203, the TS packets accumulated in the SDRAM 208 are inputted to the MPEG decoder interface 213 as

MPEG-TS data. The MPEG decoder interface 213 outputs the inputted MPEG-TS data to a demultiplexer 214. The demultiplexer 214 separates the ~~MPET-TS~~ MPEG-TS data inputted by the MPEG decoder interface 213 into video data, audio data and the like, and outputs the separated video data and audio data to a decoder 215.

Please amend the paragraph at page 26, lines 19-28 as follows:

Thus, in the CSMA/CD scheme, since the timing at which transmission and reception of the synchronization control frame are completed (that is, the timing of the transmit complete interrupt of the built-in network controller in network interface 44, and of the receive complete interrupt of the built-in network controller in the network interface 212) is simultaneous, the timing at which the synchronization master apparatus 12 resets the clock counter register 31 and the timing at which the synchronization ~~master~~ slave apparatus 13 resets the clock counter register 201 are the same.